

From,

Nalina S.B  
Asst Professor,  
Dept of ECE,  
JNNCE,Shivamogga

Date: 09.12.2020

PD

Ele  
Dev

To,

The Principal  
JNNCE,Shivamogga

Through,

The HoD  
Dept of ECE  
JNNCE,Shivamogga

Respected Sir,

**Sub: Regarding the partial delivery of lecture on the subject Electronic Devices for 3<sup>rd</sup> semester ECE students on 11.12.2020**

With respect to the subject cited above, I would like to bring to your kind information that our alumni student Mr. Sanjay A.C, Working as Design Engineer in the VLSI Analog layout field, at Cadence Design Systems, Bangalore has acknowledged to our proposal for delivering lecture on Electronic Devices for 3<sup>rd</sup> semester students. Since he is working in the VLSI sector and enormous knowledge in the same field he has plans to deliver lecture in Fabrication Technology/Integrated Electronics.

As this program will help the students in their academic as well as it will be one of the important activity under NBA Accreditation programme, I request you to please provide permission to organize this session. I hope you will kindly do the needful.

Thanks and Regards,

*Nalina*  
Nalina S.B

*Not handed*

*[Signature]*  
9/12/2020  
Head of the Department  
Electronics and Communication  
J.N.N. College of Engineering  
SHIMOGA-577 204.

*[Signature]*

09/12/2020

Compose

Inbox 3,748

Starred

Snoozed

Sent

Meet

New meeting

My meetings

Hangouts

 Nalina +

No recent chats

Start a new one



## Invitation for partial delivery

**Nalina S B** <nalinasb@jnnce.ac.in>  
to sanjayac074, HOD

Dear Sir,

We have requested you to deliver a session for the program will help the students to acquire the knowledge hereby thank you on behalf of department of ECE and JN

The session scheduled is as follows

Date: 16th December 2020

Time: 3:30PM to 4:30PM

Platform: Go to meet

Thanks and Regards

Nalina S.B  
Asst Professor



# Integrated Circuits

Sanjay A C,  
Cadence Design Systems,  
Bengaluru

# Integrated Circuits

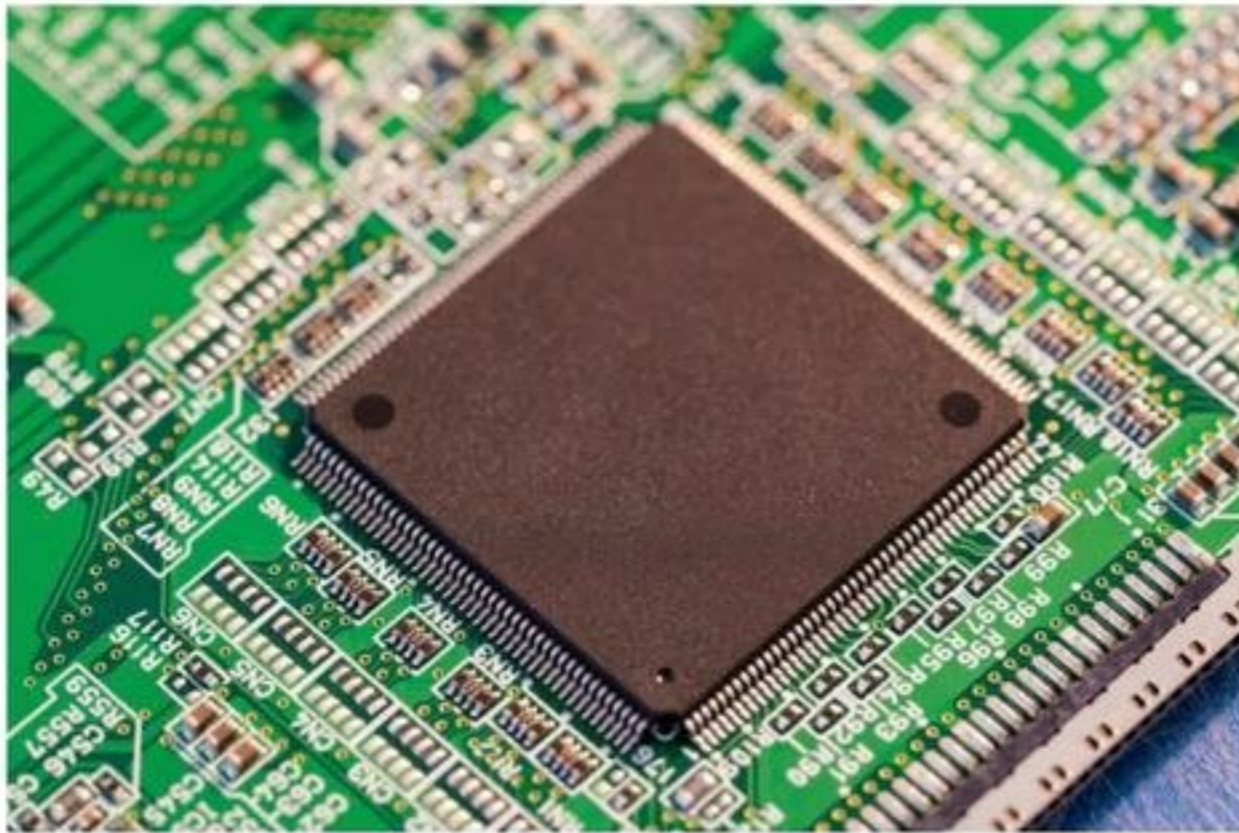
Sanjay A C,  
Cadence Design Systems,  
Bengaluru

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- ▶ IC packages
- ▶ IC design flow
- ▶ Transistor
- ▶ MOSFET
- ▶ FINFET
- ▶ FDSOI
- ▶ GAAFET
- ▶ MBCFET
- ▶ Metal structure

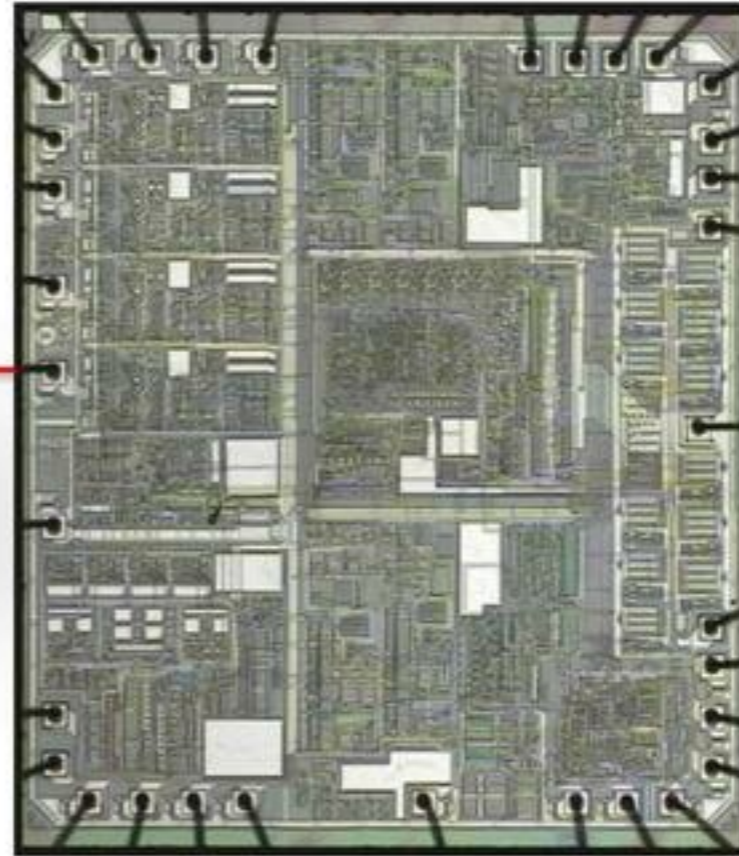
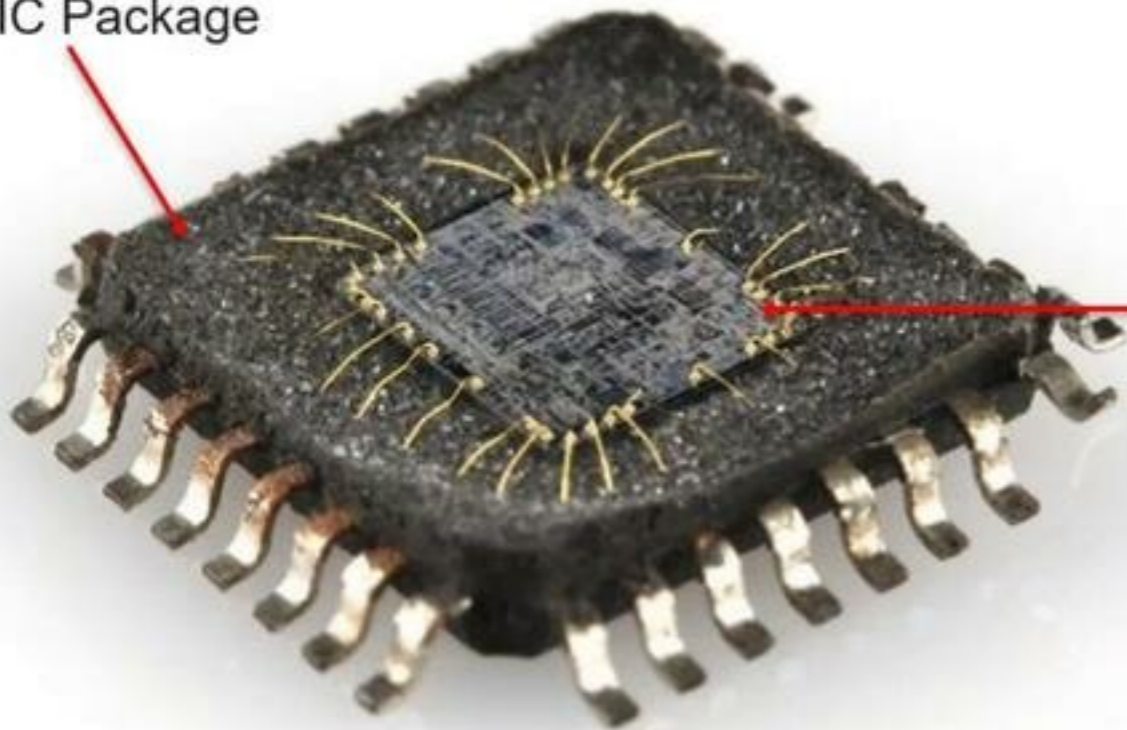
# Integrated Circuits

An **IC** is a small wafer, usually made of silicon, that can hold anywhere from hundreds to millions of transistors, resistors, and capacitors.



# Integrated Circuits

IC Package



# IC Packages

- Through-hole technology.
- Surface-mount technology.
- Chip carrier.
- Pin grid array.
- Flat **package**.
- Small Outline **Integrated Circuit**.
- Chip-scale **package**.
- Ball grid array.



# IC Packages

## IC Package - Through Hole



PDIP



DIP



ZIP



PENTAWATT



T7-TO220



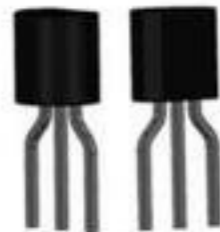
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TO92



TO18



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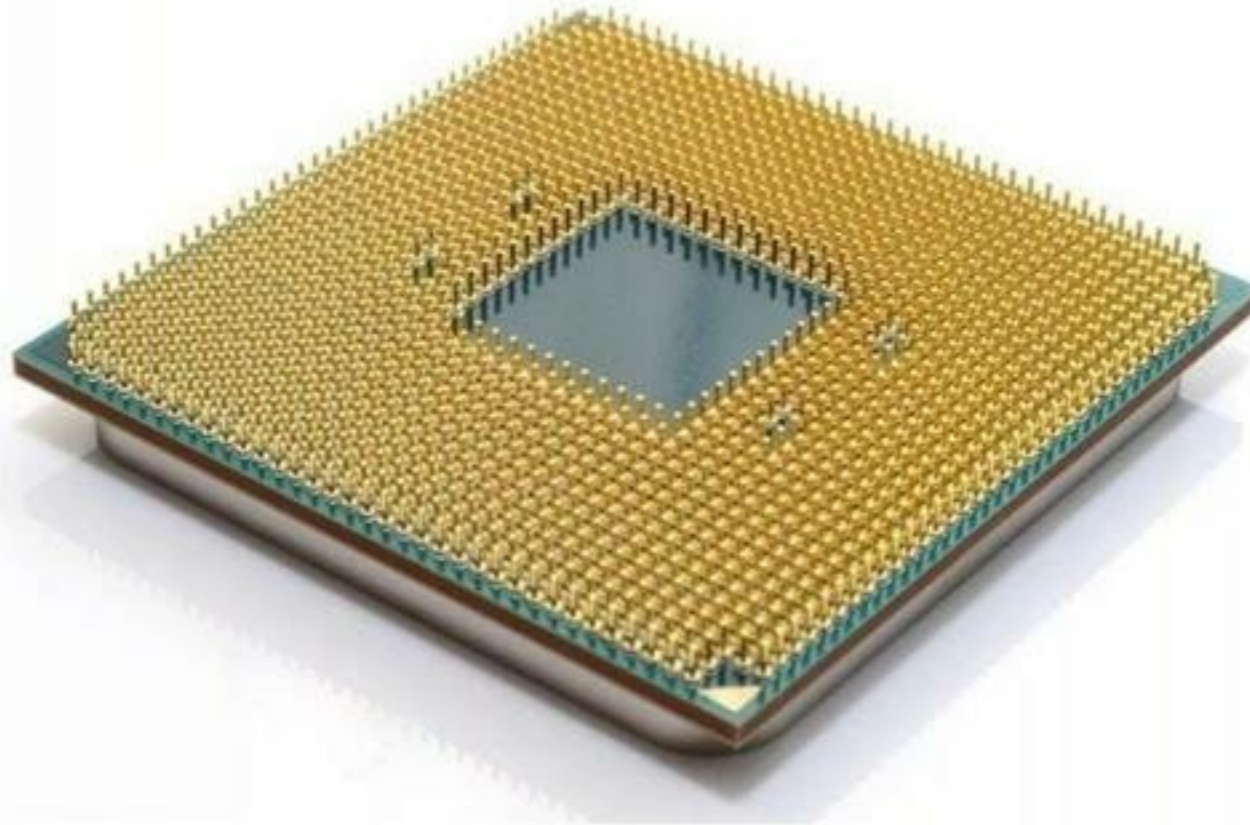
# IC Packages

## IC Package - Surface Mount

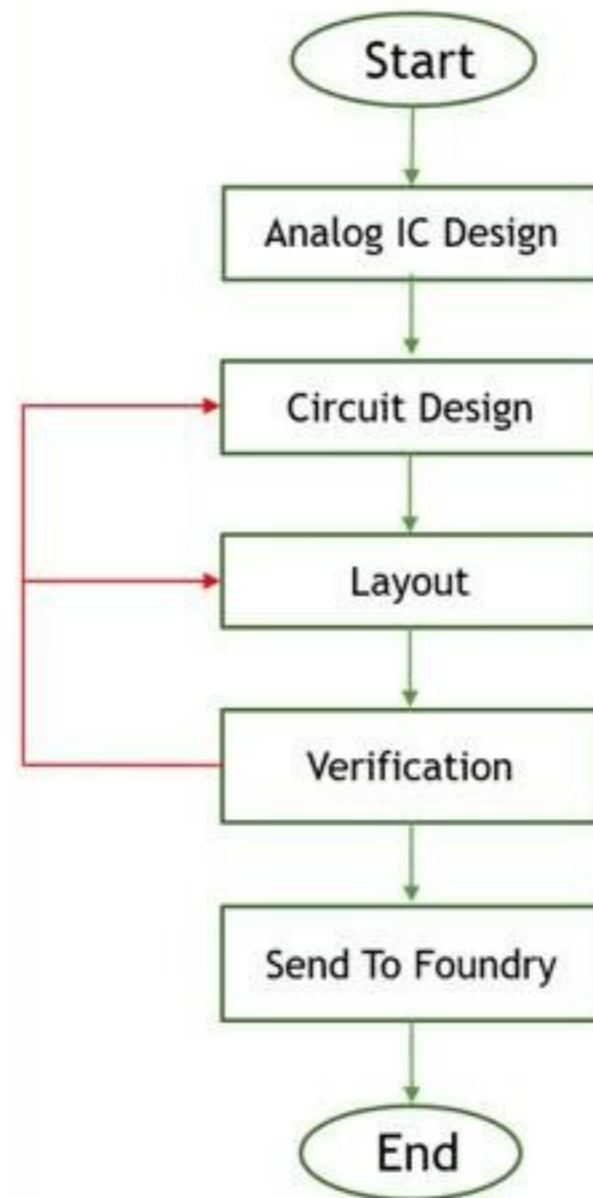


# IC Packages

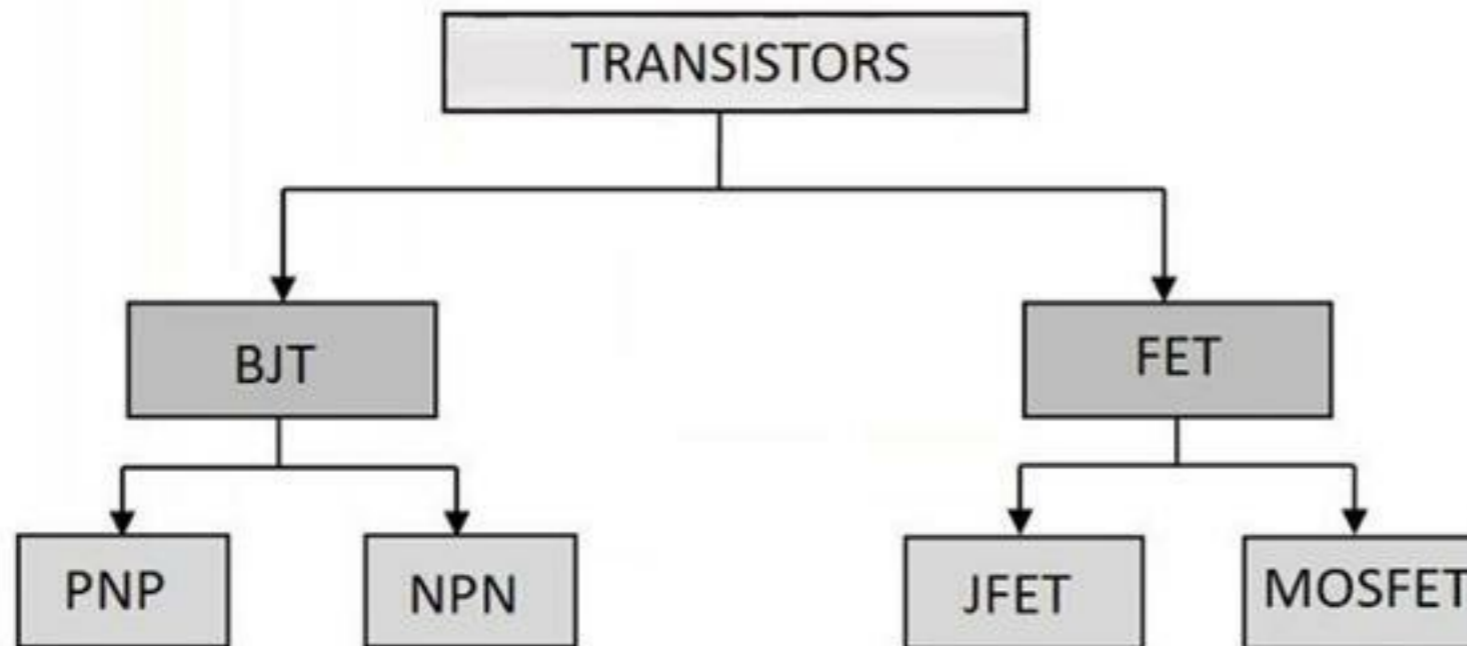
Pin grid array



# IC Design Flow:



# Transistors

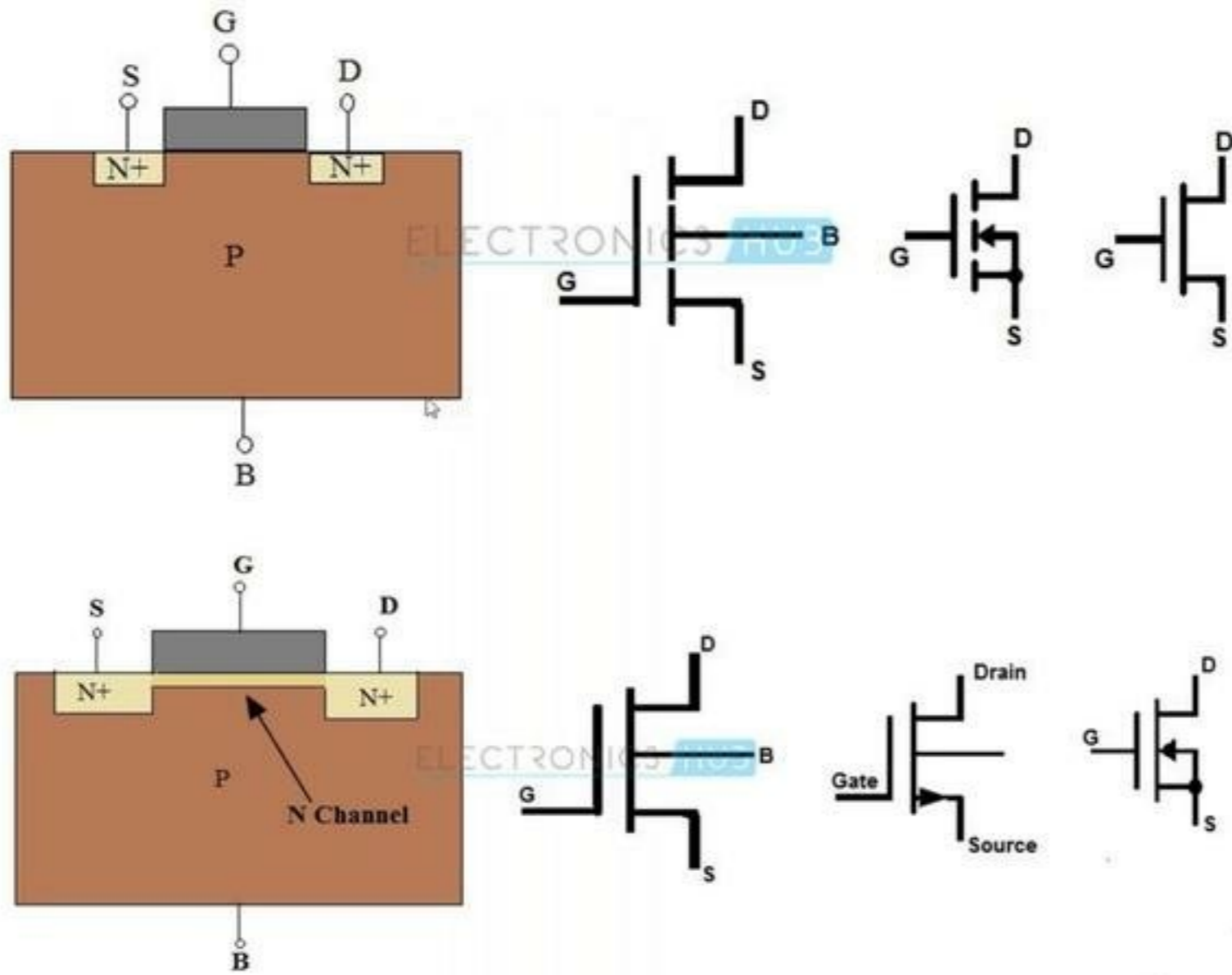


# MOSFET

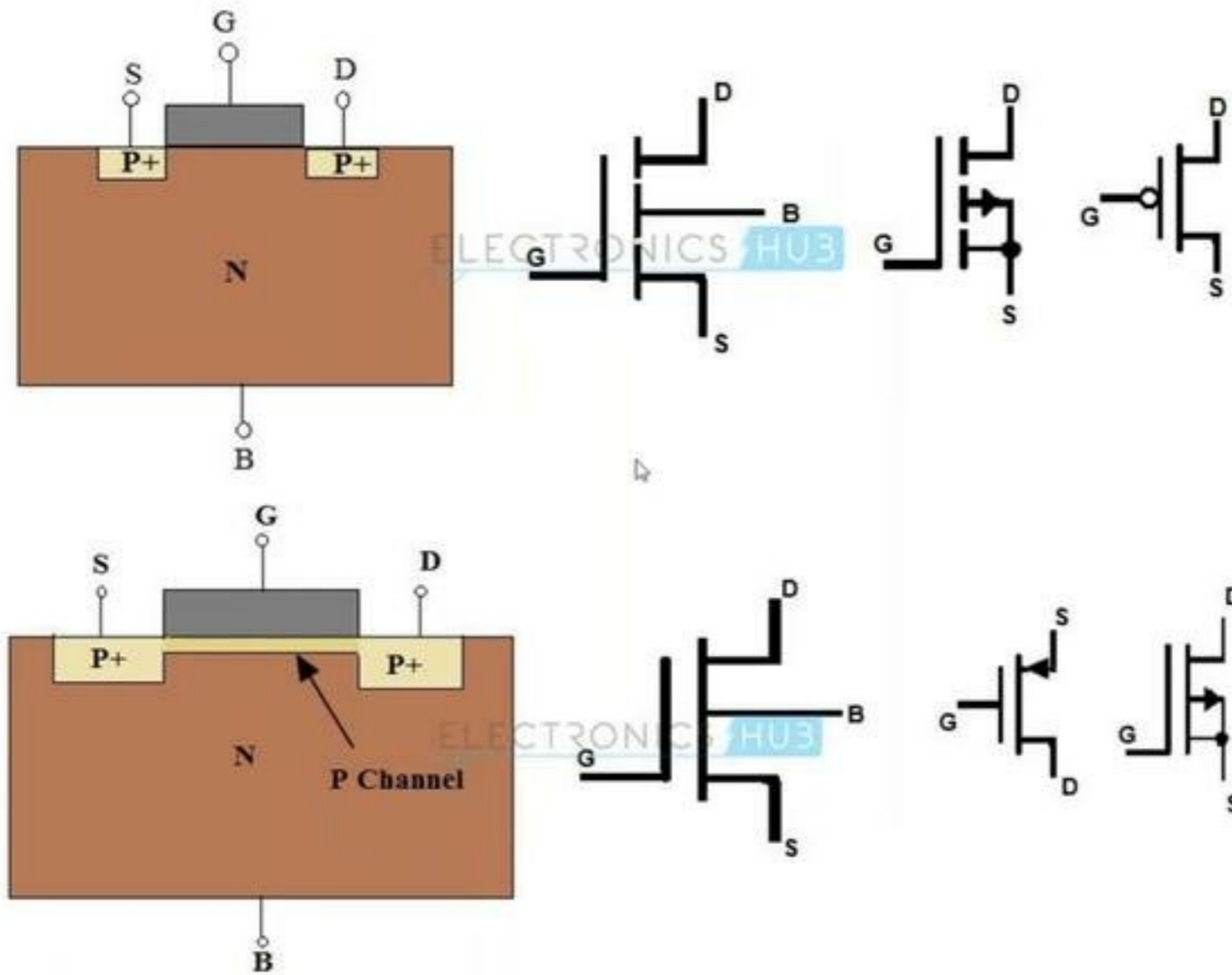
Metal Oxide Semiconductor Field Effect Transistor

- ▶ We have two types of MOSFET
  - ▶ NMOS - N channel MOSFET
  - ▶ PMOS - P channel MOSFET

# NMOS

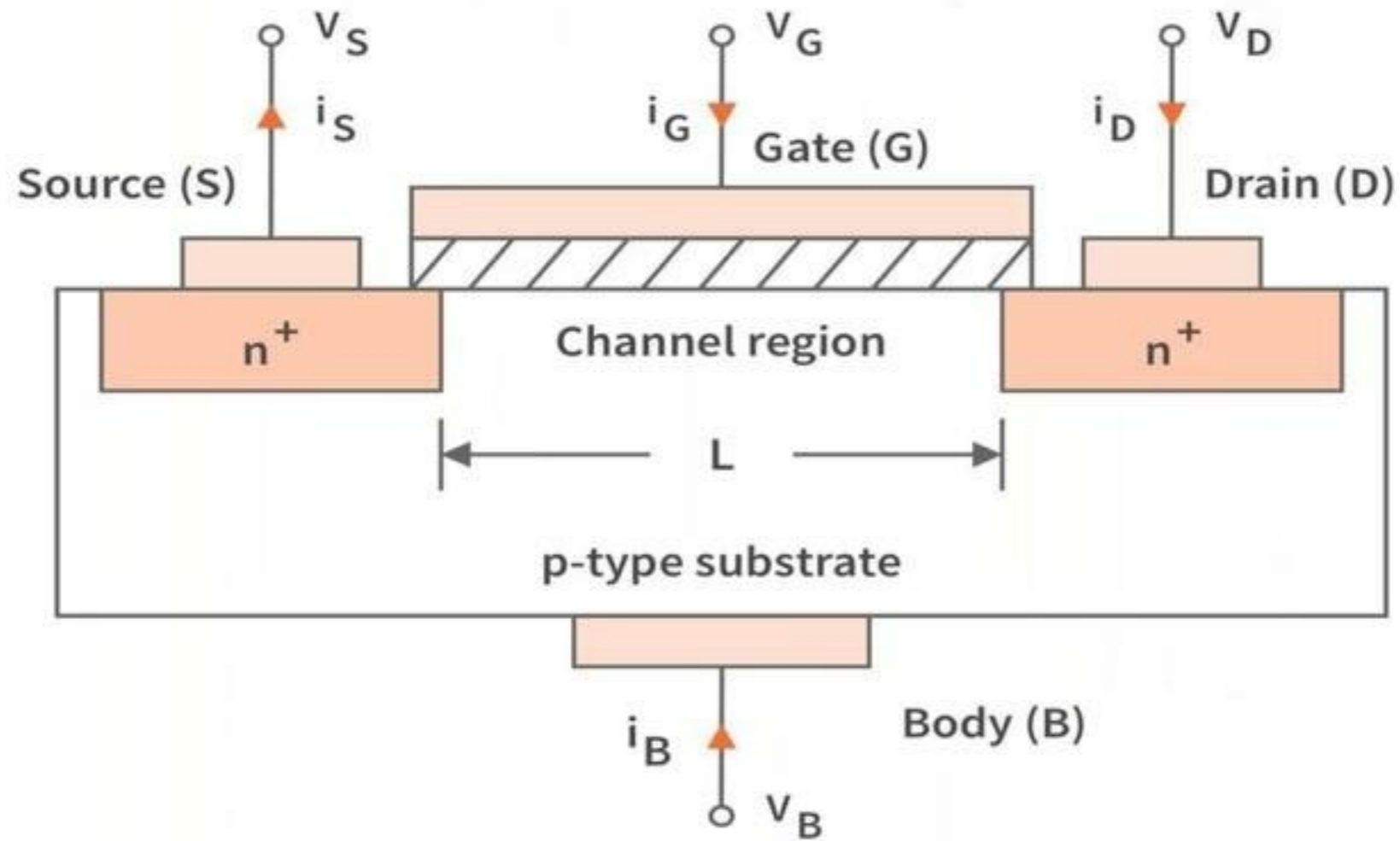


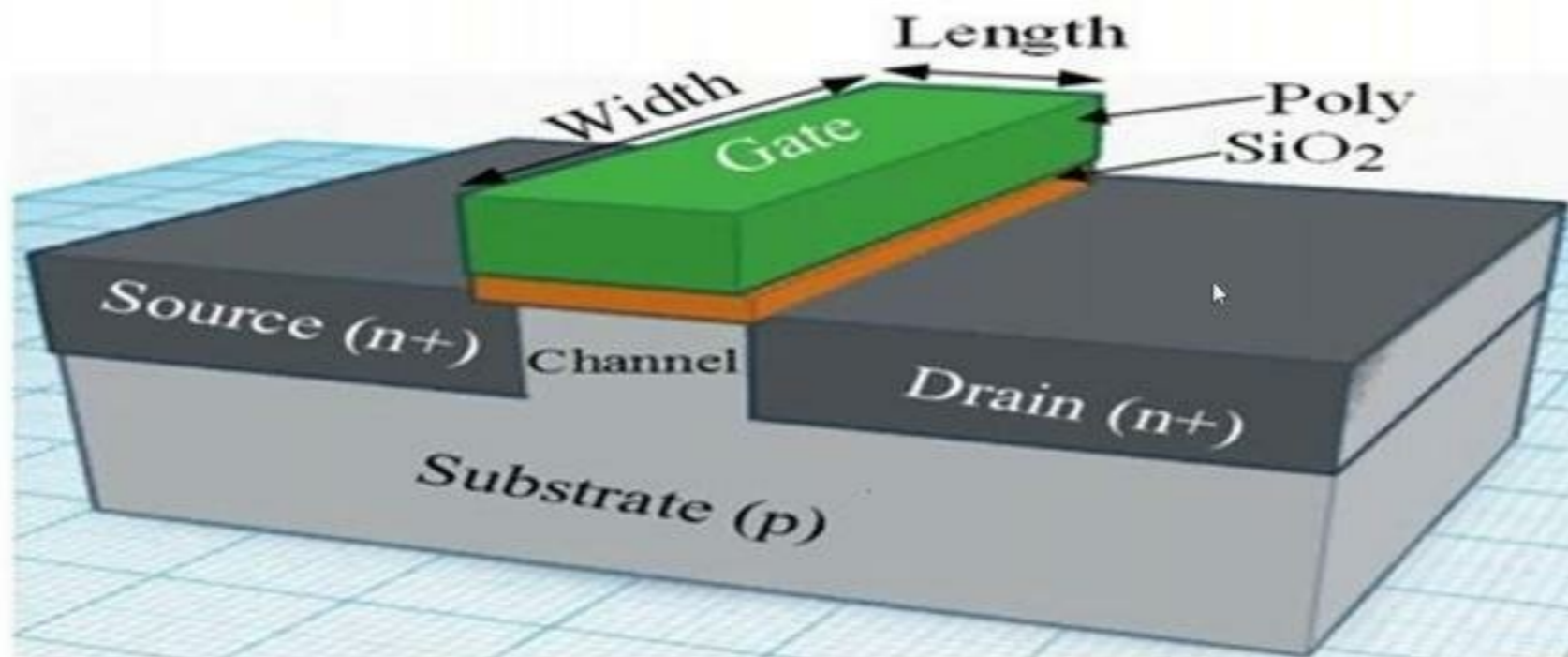
# PMOS





## NMOS - Negative Channel Metal Oxide Semiconductor

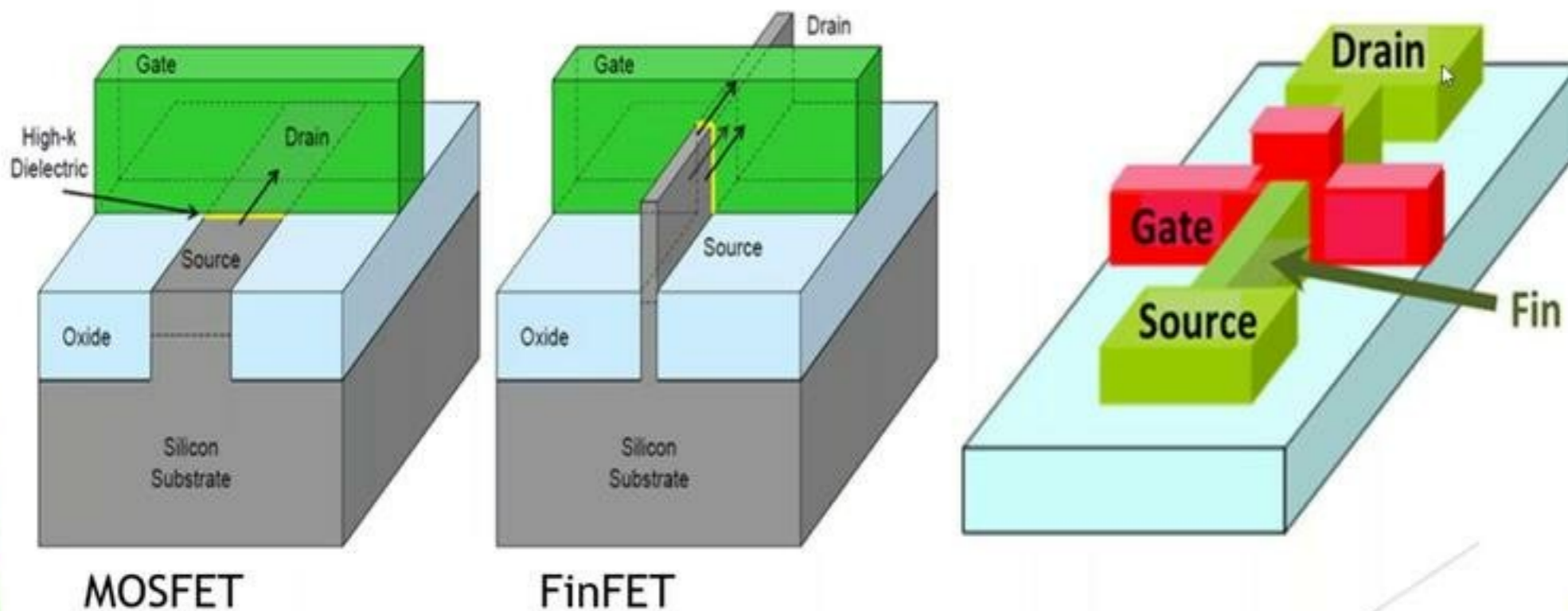


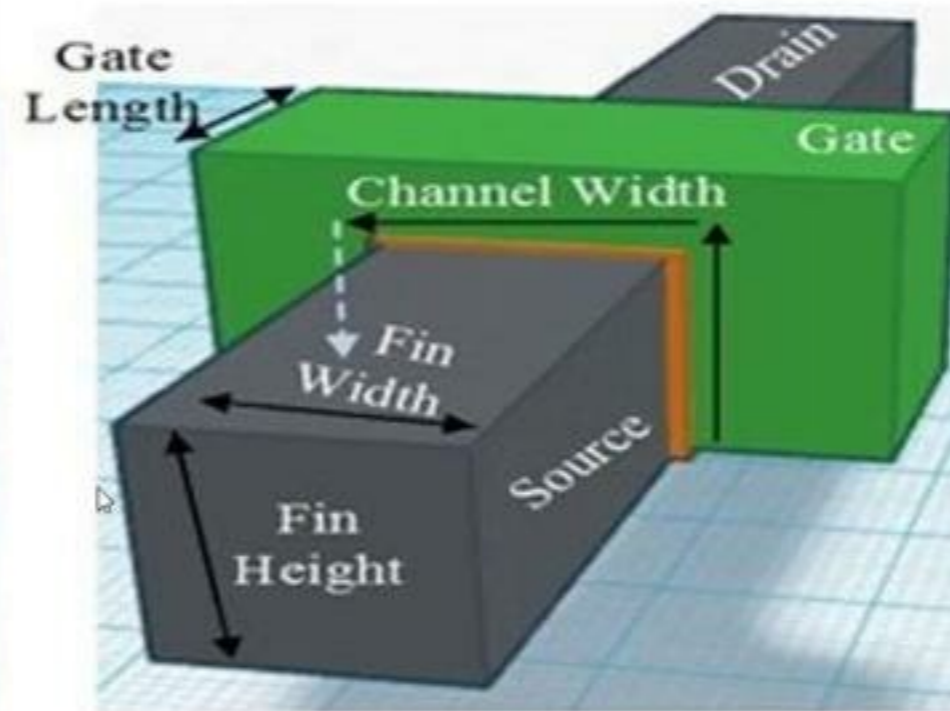
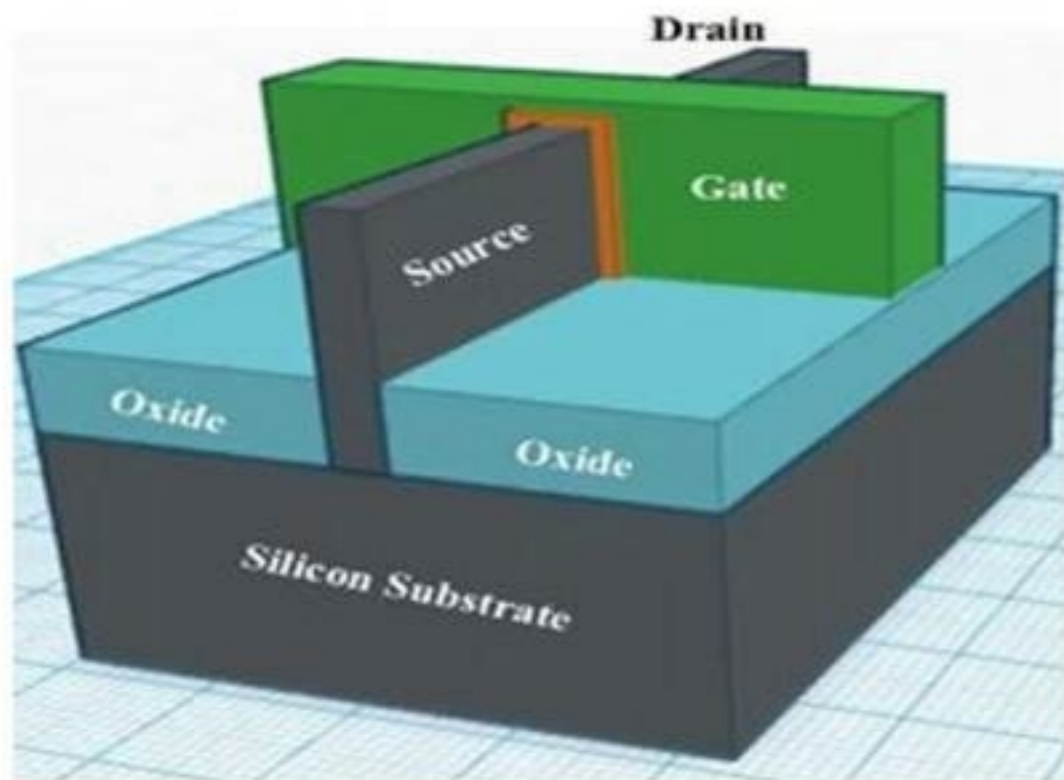


3D view of NMOS.

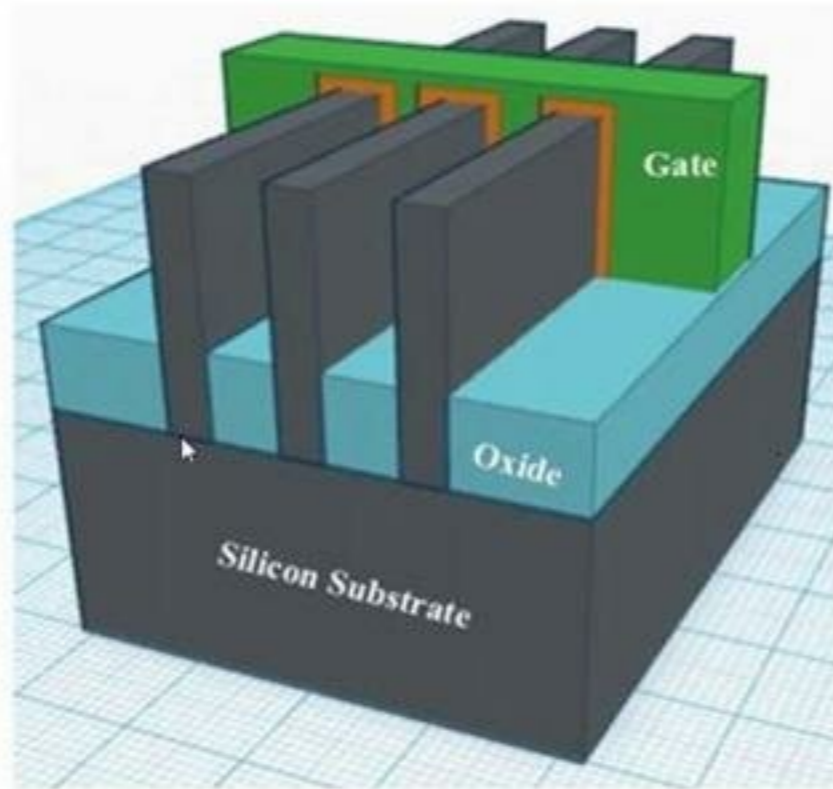
# FinFET

- Full form -> Fin field-effect transistor
- Source and drain region resembles the fin on the silicon surface
- In panner MOS, the channel is **horizontal**. While in FinFET channel, it is **vertical**
- Mainly used for technologies beyond 28nm





In FinFET drive current can be increased by increasing the width of the channel that is by increasing the height of the Fin.



Constructing parallel multiple Fins connected together to increase the device drive current.

## Advantages of FinFET:

- Higher drive current
- Higher speed
- Low leakage
- Low power consumption
- FinFET suffers less from dopants-induced variation
- Scaling of the transistor beyond 28nm

## SOI(Silicon-On-Insulator):

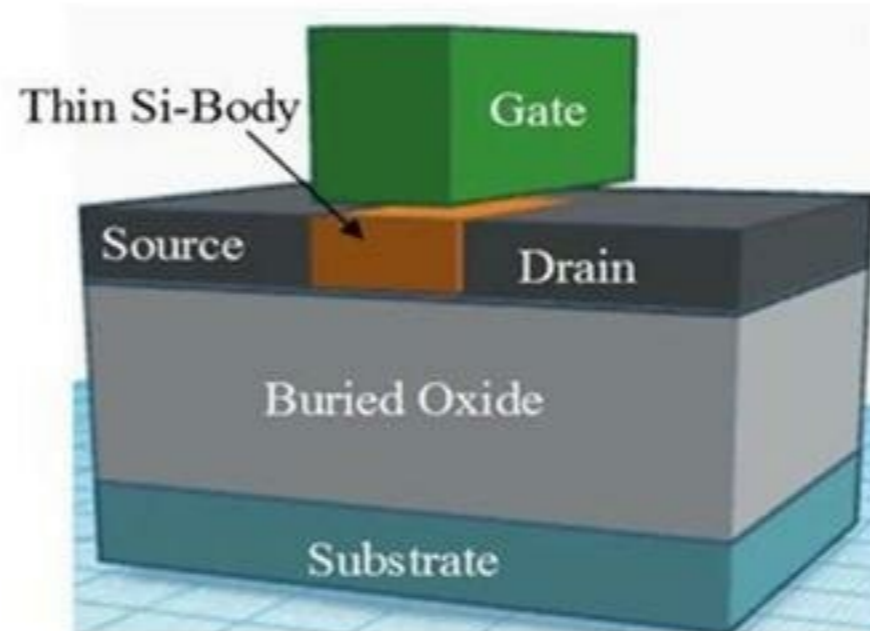
It has three layers:

1. Thin surface layer of silicon(where transistor are formed)
2. An underlying layer of insulating material
3. A support or “handle” silicon wafer



## Types:

- Partially Depleted SOI(PDSOI)
- Fully Depleted SOI(FDSOI)

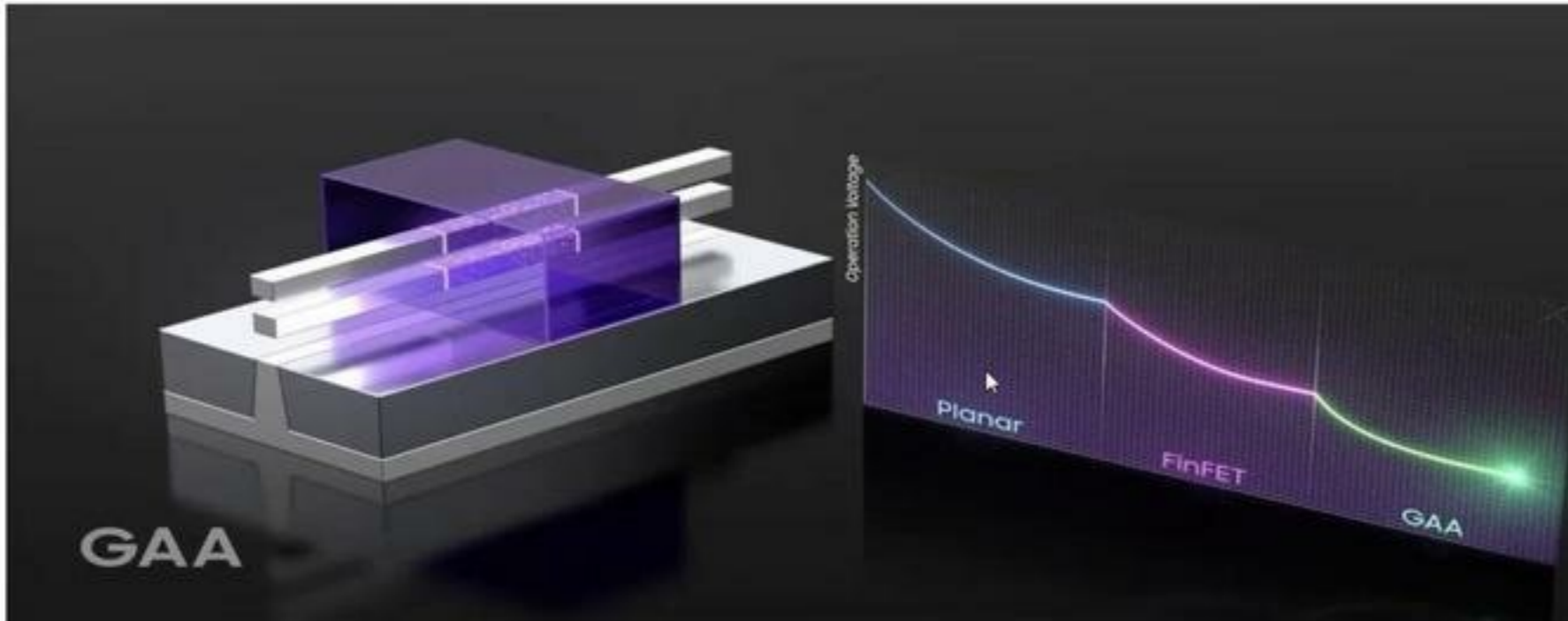


# Advantages of FDSOI

- ▶ Improved speed
- ▶ Reduced power
- ▶ Simpler manufacturing process
- ▶ It delivers a good power, performance, cost tradeoff compared to both bulk and FinFET technologies

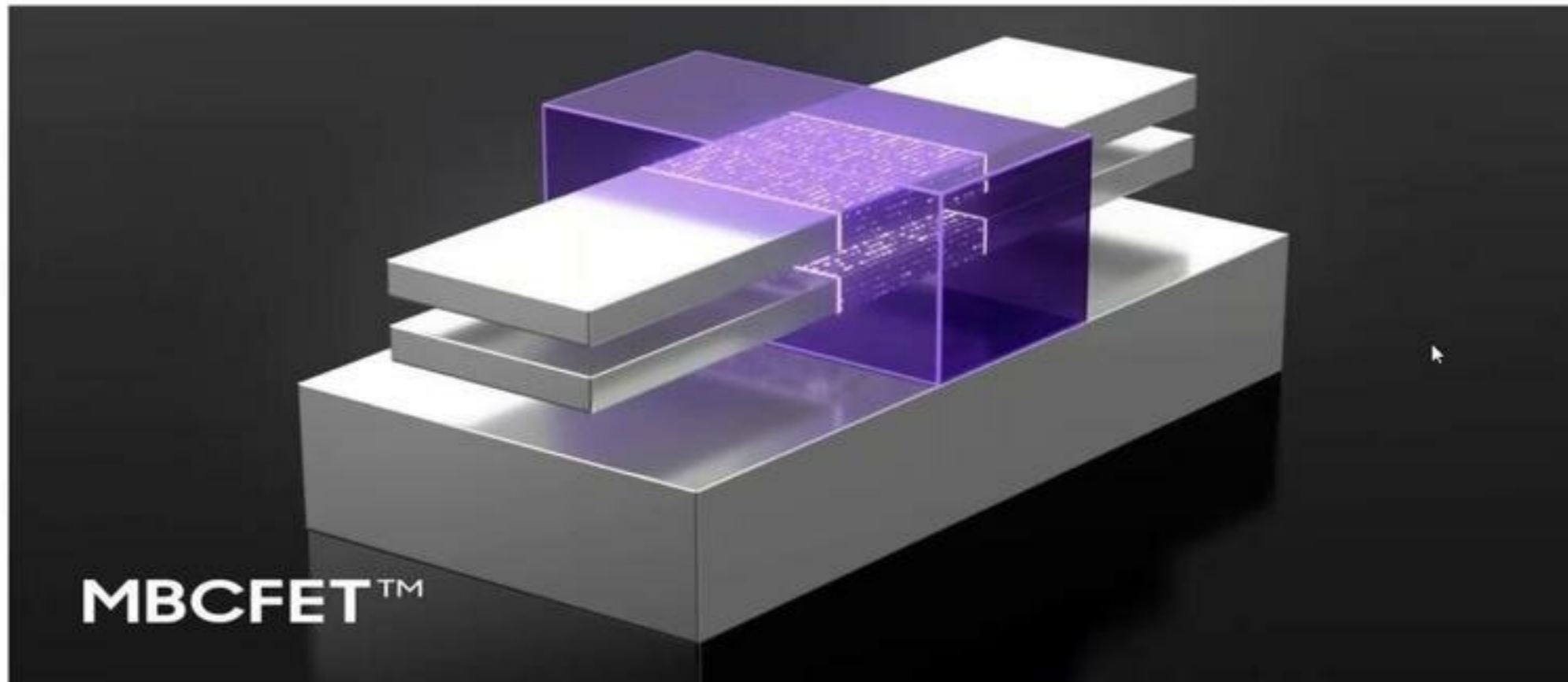


## GAAFET(Gate All Around FET):

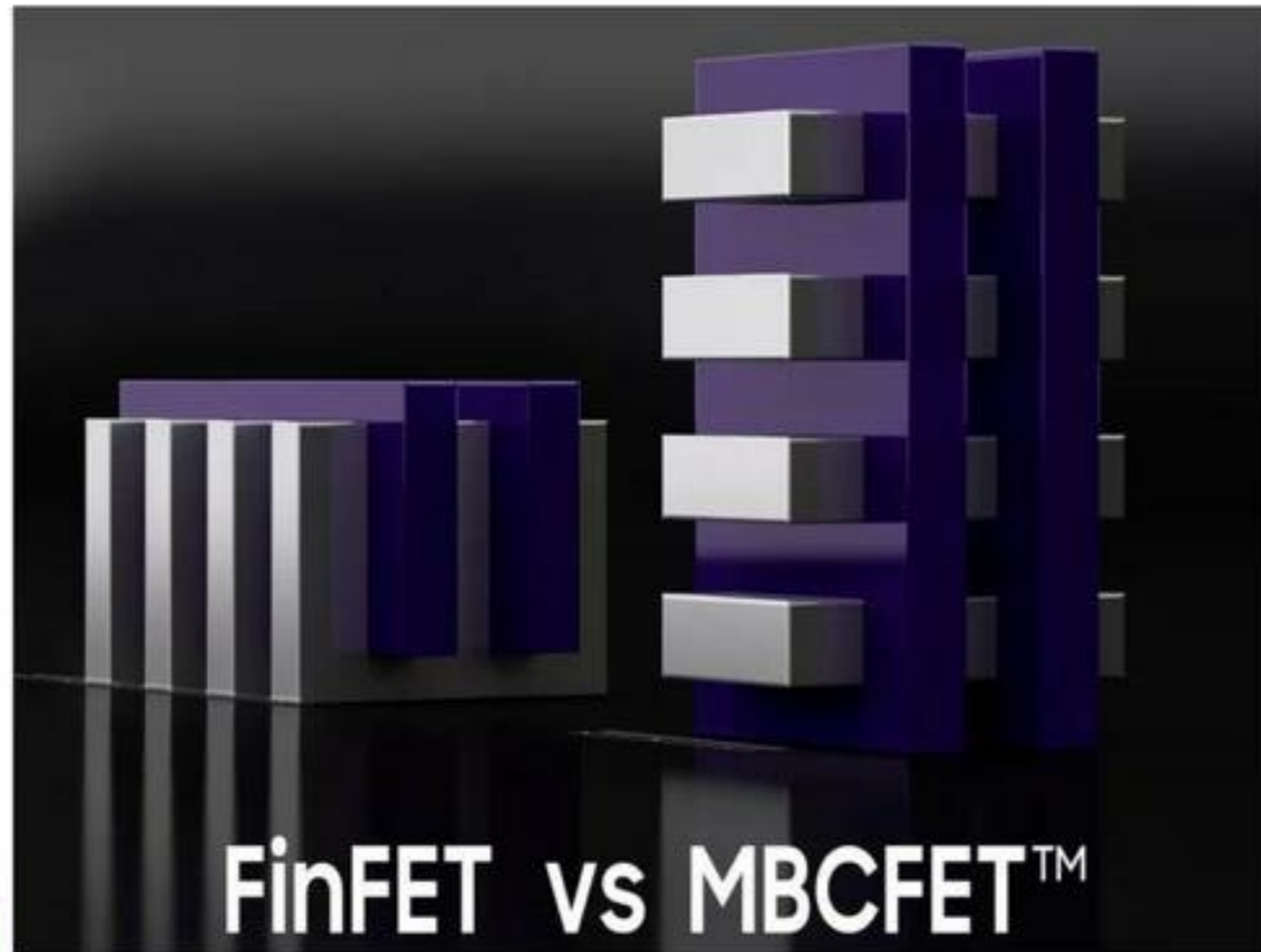


- Due to the process node becoming smaller and smaller, electrostatic effects started to cause problem
- A solution was to use GAA nanowires to limit those effect
- But nanowires are apparently really hard to integrate into silicon

## MBCFET (Multi-Bridge Channel FET):

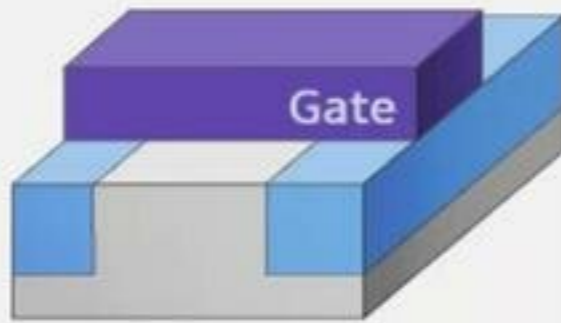


Samsung using thin layers (nanosheets) instead of nanowires enabling greater current per track.

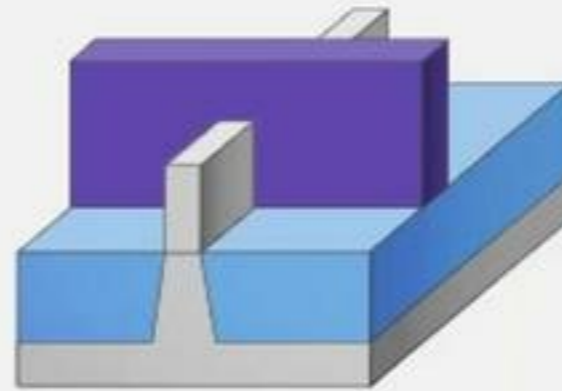


- MBCFET will enable manufacturing of chips using a 3nm process
- Compared to 7nm FinFET technology, Samsung's 3GAE/MBCFET process should provide up to a 45% reduction in chip area with either 50% lower power consumption or 35% higher performance

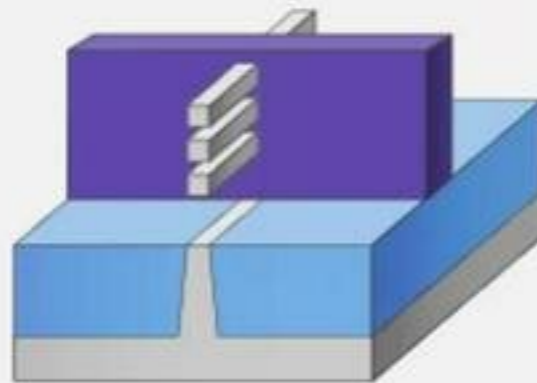
# FETs



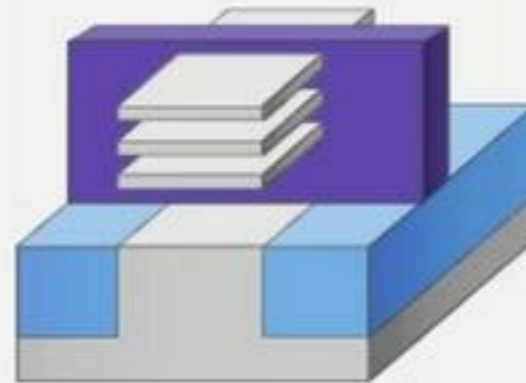
Planar FET



FinFET

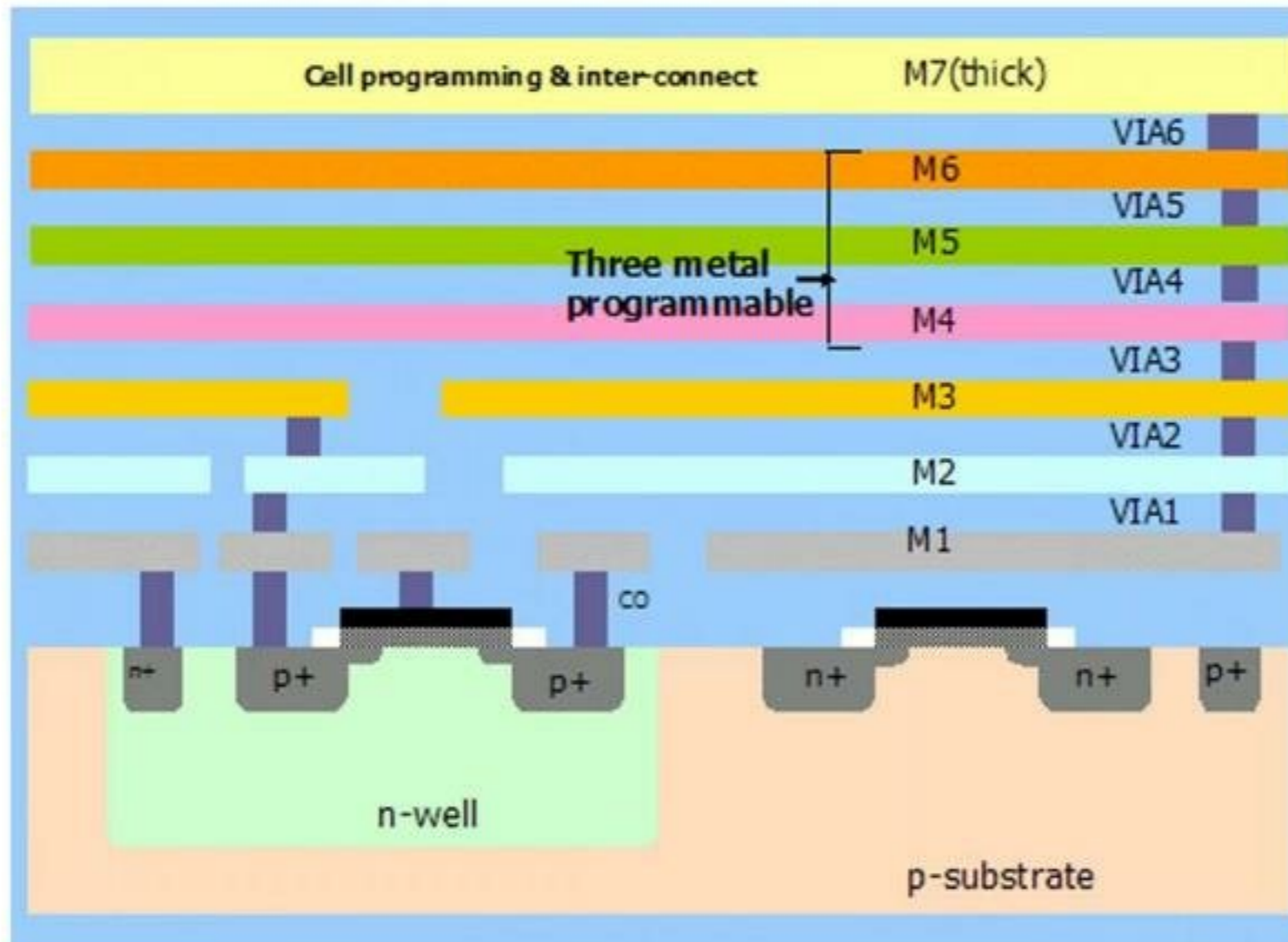


GAAFET  
(Nanowire)

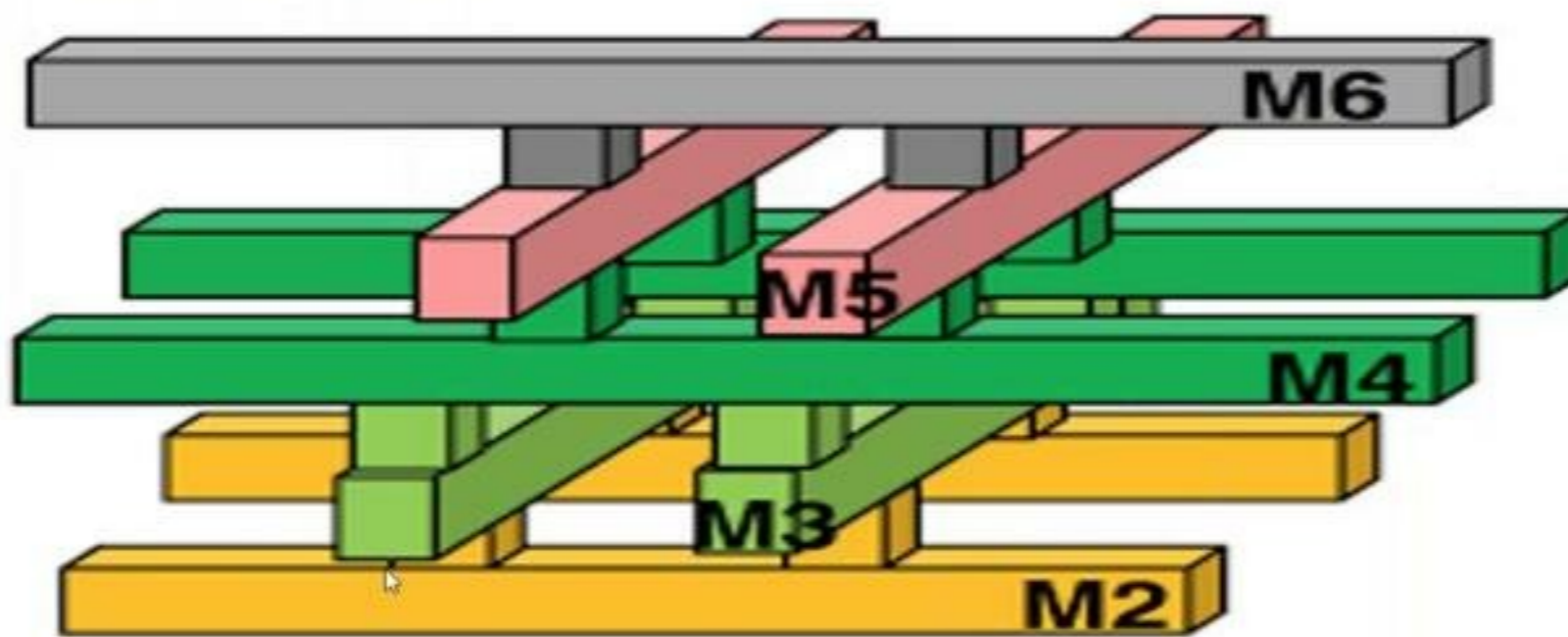


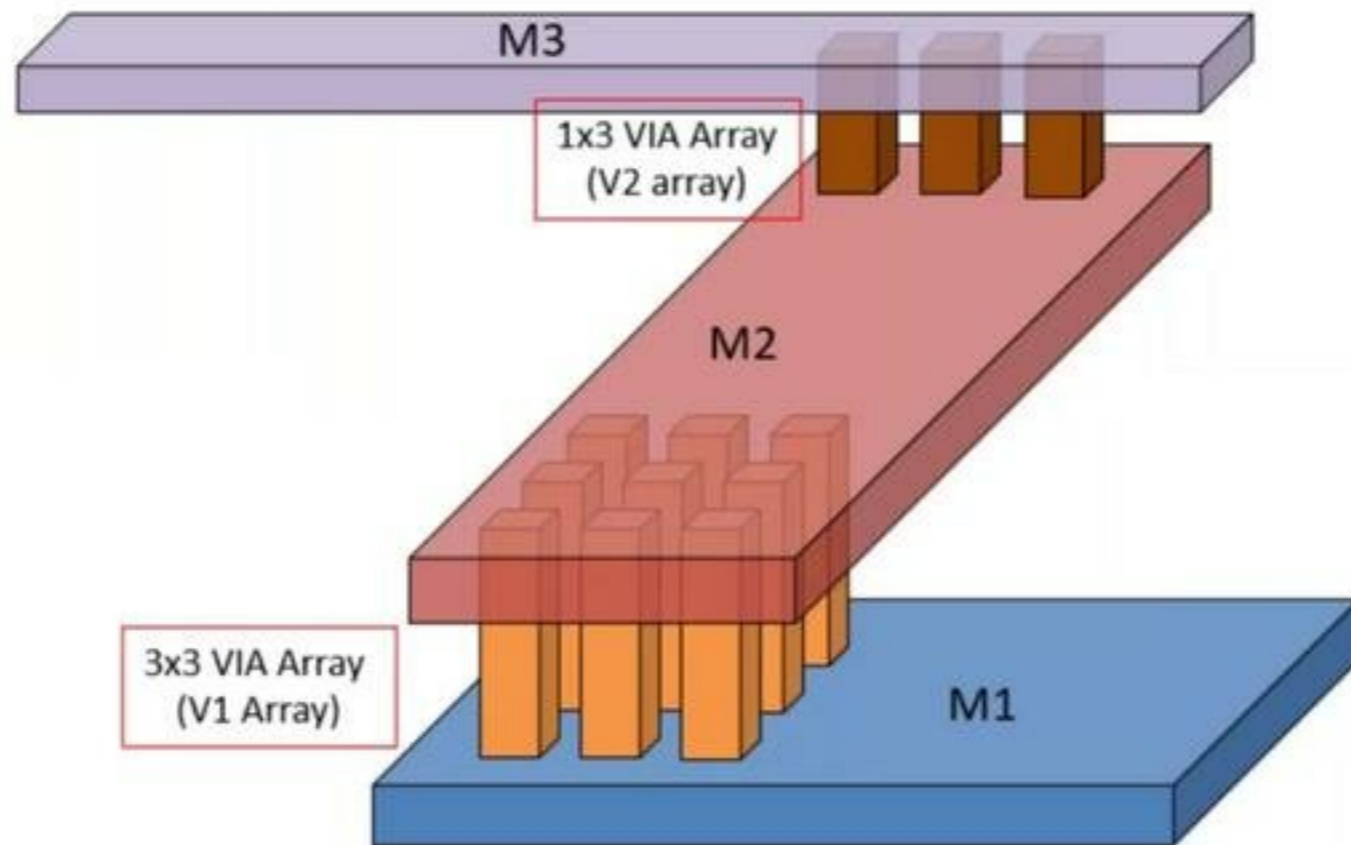
MBCFET™  
(Nanosheet)

# Metal Structure



# Metal Structure





3D View of VIA and Metal Connection.

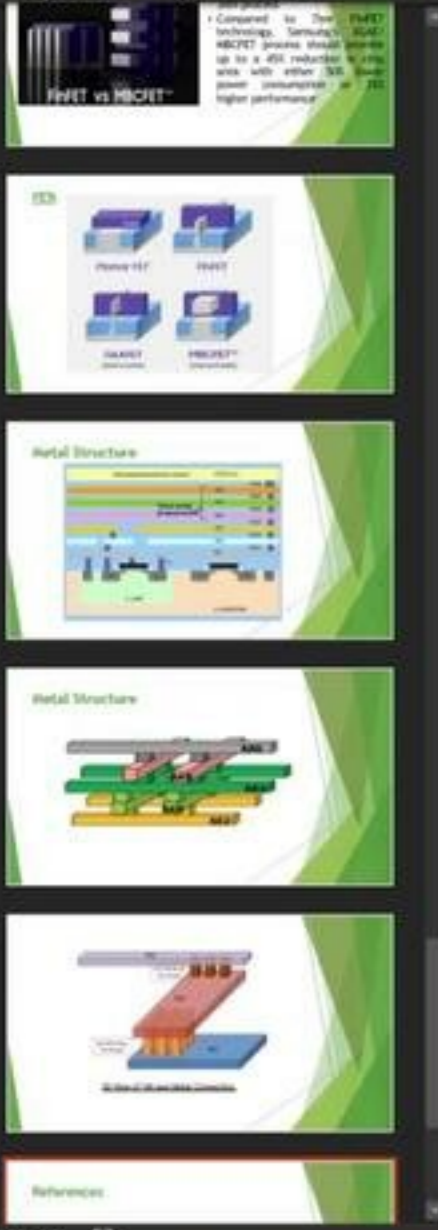
# References

- ▶ <https://youtu.be/3otqUu-7WUQ>
- ▶ <https://www.design-reuse.com/articles/41330/cmos-soi-finfet-technology-review-paper.html>
- ▶ <https://www.coventor.com/blog/everything-you-need-to-know-about-fdsoi-technology-advantages-disadvantages-and-applications-of-fdsoi/>



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Clipboard Slides Font Paragraph Drawing Editing Voice Webex



# References

- ▶ <https://youtu.be/3otqUu-7WUQ>
- ▶ <https://www.design-reuse.com/articles/41330/cmos-soi-finfet-technology-review-paper.html>
- ▶ <https://www.coventor.com/blog/everything-you-need-to-know-about-fdsoi-technology-advantages-disadvantages-and-applications-of-fdsoi/>

# Industrial talk on Electronic Devices Attendees

## Summary

### Meeting Date

December 16, 2020 3:07 PM IST

### Meeting Duration

78 minutes

### Number of Attendees Meeting ID

91 454-432-061

## GoToMeeting

## Details

Name	Email Address	Join Time	Leave Time	Time in Session (minutes)
4JN18EC018 BHAVANA K		3:31 PM	3:56 PM	25
4JN19EC004 ACHARYA VINAY VASUDEVA		3:34 PM	4:06 PM	31
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4JN19EC010 AJITH A M		3:47 PM	4:24 PM	36
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4JN19EC073 RADHIKA.K.S.	radhikaradhika38193@gmail.com	3:30 PM	4:24 PM	54
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