National Education Society (R.)

Jawaharlal Nehru New College of Engineering, Shivamogga

(Approved by AICTE, New Delhi, Certified by UGC 2f & 12B, Accredited by NAAC –'B', Accredited by NBA, Recognized by Govt. of Karnataka and Affiliated to VTU, Belagavi)

Department of Electronics & Communication Engineering

No.JNNCE/ECE/1097/2021-22

Date: 05/01/2022

Submitted to the Principal:

Through, HOD, ECE Dept, JNNCE, Shimoga

Department of Electronics & Communication Engineering JNNCE SHIVAMOGGA-577 204

Subject: Approval for remuneration towards partial delivery

With reference to the above subject the department of Electronics and Communication has conducted the Invited Lecture on the topic **"Digital Signal Processors Architecture"** in the course Digital Signal Processing for 5th semester students during 29/12/2021 & 30/12/2021. This Invited Lecture is planned under the theme "Partial Delivery of the curriculum by Industry Professional". Mr Paalchandra (Senior Technical Lead), Path Partner Technology, Bangalore was invited as the recourse person for the Lecture. In this regard, it has been planned to provide remuneration of Rupees 3000/- towards this Invited Lecture conducted during the above said days. Approval is requested to sanction the remuneration for the resource person and do the needful.

Course coordinators

Sharath S M & Smitha S M

Head of the Department 5/1/22

Dr S V Sathyanarayana
Head of the Department
Electronics and Communication
J.N.N. College of Engineering
SHIMOGA-577 204.

ENCL: Request letter to the resource person

Email conversation for acceptance

Forwarded. Conducted for two days

5/1/22

Professor & Dean (Academic)
J.N.N. College of Engineering
Nehrule, Sagar Road,
Shivamogga - 577 204.

Yes

6-1-22

Principal
Jawaharlal Nehru National
College of Engineering, Shivamogga.

Gmail

Smitha S M <smithasm@jnnce.ac.in>

Partial delivery on Digital Signal Processor

2 messages

Smitha S M <smithasm@jnnce.ac.in>
To: mvp.bhat@gmail.com
Cc: Sharath S M <sharathsm@jnnce.ac.in>

Thu, Dec 9, 2021 at 3:21 PM

Good afternoon sir, with respect to partial delivery of the Digital Signal Processing course on Digital Signal Processor(Module 5) I am hereby attaching the schedule . Please find the attachment.

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With Regards,

Smitha S M,
Assistant Professor,
JNNCE,
Shimoga.

E & C Program is Accredited by NBA for the period 1.7.2019 to 30.6.2022

JNNCE (Estd. 1980)
Accredited by NAAC 'B' & Certified by UGC 2f & 12B
2018-2019 Rankings:
Outlook: 48th (India); 7th (Karnataka);
** India Today: 34th (India); 7th (Karnataka);*
** The Week: 31st (India);20th (South India) ;11th (Karnataka);*
**Times Magazine 118th (India), 11th (Karnataka)*
**Chronicle 18th (India) ; A+ Grade*
** Career 360: AAA*

Vision of Electronics & Communication Department

To be a premier centre of education and research in Electronics & Communication Engineering for producing competent engineers to cater to the needs of industry and society.

Mission of Electronics & Communication Department

M1: Impart quality education through innovative and continuous teaching – learning process

M2: Groom the students with required foundations of Electronics & Communication Engineering and inculcate in them the professional ethics & human values.

M3: Train the students and the faculty in state – of – the-art technologies and motivate them for higher studies & innovation based research for the needs of the industry and society.

M4: Create centers of excellence in the field of Electronics & Communication Engineering in collaboration with the industries and academic organizations.

09-12-2021.pdf
318K

palachandra mathur venkataraju <mvp.bhat@gmail.com>
To: Smitha S M <smithasm@jnnce.ac.in>
Cc: Sharath S M <sharathsm@jnnce.ac.in>

Thu, Dec 16, 2021 at 11:38 AM

National Education Society (R.)

Jawaharlal Nehru New College of Engineering, Shivamogga

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Department of Electronics & Communication Engineering

Ref.No.JNNCE/ECE/1089

PD Digital Proce T-3-

To,

Mr. Palachandra M V
Senior Technical Lead
Path Partner Technology

Dear Sir,

In continuation with the telephonic conversation with you, we are happy to invite you to deliver an **"Invited Lecture"** on Digital Signal Processing course and the topic is **"Digital Signal Processors"** for 5th semester students. This is a part of lecture series by industry professionals. Hence, we here by request you to be resource person and schedule is as follows,

Sl. No.	Date & Time	Semester & Section
1.	18-12-2021 & 09:00AM to 11:00AM	5th Sem, A & B Sec
2.	08-01-2022 & 09:00AM to 11:00AM	5th Sem, A & B Sec

Thank you.

JNNCE SHIVAMOGGA-

Head of the Department 9/12/21

Dr. Sathyanarayana S. V.

Organizers:

Mr. Sharath S M
Ms. Smitha S M
Assistant Professors,
Department of ECE.
JNNCE, Shivamogga