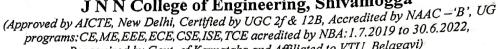


J N N College of Engineering, Shivamogga



Recognized by Govt. of Karnataka and Affiliated to VTU, Belagavi) Departmentof Electronics & Communication Engineering



Report on "Invited Lecture"

"Semiconductor Memories and Testing & Verification"

JNNCE. The Department of Electronics and Communication Engineering, Shivamogga had organized an invited lecture on "Semiconductor Memories and Testing & Verification" for final year students as a part of industrial professional interaction on 29th November 2021.

The session started with the introduction about the industry person Mr. Sachinkumar K, Digital Design Engineer, Intel India Pvt. Ltd. which was delivered by Ms. Shwetha H R.

In this session, he explained about semiconductors memories, Introduction to semiconductor memories & its usage. The memory has been classified into 2 types of RAM and ROM, RAM is classified into 2 types DRAM and SRAM. ROM is divided EPROM, PROM, and Masked Memories.

Then the speaker guided the students how to crack core company interviews, also motivated the students how to face the challenges in life and how to settle in life with the high position and high salary. He also encouraged students by giving the live examples of our seniors who passed out from JNNCE and are in good position.

It was a wonderful and useful session for our students delivered by industry expert.

Ms. Shwetha H.R.

Assistant Professor.

Department of ECE.

JNNCE, Shivamogga

Dr. Sathyanarayana S. V

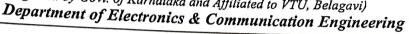
Professor & Head Department of ECE JNNCE, Shivamogga



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To.

Date:28-11-2021

Mr. Sachinkumar K. Digital Design Engineer Intel India Pvt. Ltd.

Dear Sir.

In continuation with the telephonic conversation with you, we are happy to invite you to deliver an "Invited Lecture" on VLSI Design course and the topic is "Semiconductor Memories and Testing & Verification" for 7th semester students. This is a part of lecture series by industry professionals. Hence, we here by request you to be resource person and schedule is as follows,

Sl. No.	Date & Time	
1		Semester & Section
2	29-11-2021 & 10:30 AM to 01:30 PM	7 th Sem, B Sec
<u> </u>	29-11-2021 & 02:30 PM to 05:30 PM	7 th Sem, A Sec
		7 Dolli, A DCC

Thank you.

Organizer:

Ms. Shwetha H.R. Assistant Professor, Department of ECE. JNNCE, Shivamogga shwethahr@innce.ac.in

Ph: 7204443953

Head of the Department

Dr. Suthyaharavaha Separtment Electronics and Communication J.N.N. College of Engineering SHIMOGA-577 204.

From: Shwetha H R <shwethahr@jnnce.ac.in> Sent: Sunday, November 28, 2021 8:44 PM To: K, Sachinkumar <sachinkumar.k@intel.com> Cc: HOD ECE < hod_ece@jnnce.ac.in>

Subject: Invitation as a resource person for "Invited Lecture"

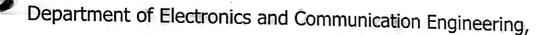
As the telephonic conversation with you, I am happy to invite you as a resource person for the "Invited Lecture" on the VLSI Design course for final year

Please find the attached Invitation and Syllabus.

With Regards,

Shwetha H R,

Assistant Professor,



JNN College of Engineering,

Navule, Shivamogga, Karnataka-577204

Ph No: 7204443953





Invitation as a resource person for "Invited 3 messages

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Shwetha H R <shwethahr@jnnce.ac.in>

Cc: HOD ECE <hod_ece@jnnce.ac.in>

As the telephonic conversation with you, | am happy to invite you as a resource person shwetha HR <

Please find the attached Invitation and Syllabus.

With Regards, Shwetha H R.

Department of Electronics and Communication Engineering,

JNN College of Engineering,

Navule, Shivamogga, Karnataka-577204

Ph No: 7204443953

Cc: HOD ECE <hoo Subject: Invitation

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Mr.Sachin-Industry-Institution-Intraction-Invitation-Letter.pdf 161K

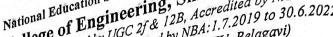
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K, Sachinkumar < sachinkumar.k@intel.com> To: Shwetha H R <shwethahr@jnnce.ac.in>

Sun, Nov 28, 2021 at 10:39 PM

Hello Madam.

I'm happy to receive this Invitation and will surely come to do lecture on VLSI design







Testing & Verification"

Semester: 7-CBCS (A Sec)

Course: VLSI Design (18EC72)

Industry Person: Mr. Sachinkumar K.

Time: 02:30 PM - 05:30 PM

Faculty: Ms. Shwetha H. R.

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JNN College of Engineering, Shivamogga

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Department of Electronics & Communication Engineering

"Invited Lecture on Semiconductor Memories and Testing & Verification"

Semester: 7-CBCS (A Sec)

Course: VLSI Design (18EC72)

Industry Person: Mr. Sachinkumar K.

Date: 29 Nov 2021

Time: 02:30 PM - 05:30 PM

Faculty: Ms. Shwetha H. R.

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Department of Electronics & Communication Engineering



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33	4JN18EC041	KIRAN C N	P	
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Department of Electronics & Communication Engineering

l. No	USN	Name	Present/Absent
5	4JN18EC056	NIKHITHA YADAV N	
6	4JN18EC057	NIRANJANA JOIS H C	P
47	4JN18EC058	PAVANA P KULAL	P
48	4JN18EC060	PRAMOD R	P
49	4JN18EC061	PRATHEEK K Y	A
50	4JN18EC066	RAJAT KUMAR	A
51	4JN18EC070	RAVIKUMAR G K	P
52	4JN18EC115	VINUSHA K	A
53	4JN18EC121	GAGANA H M	P
54	4JN18EC122	SANTHOSH M S	P
55	4JN18EC124	ADITHYA T R	P
56	4JN19EC400	ADARSHA D M	
57	4JN19EC401	AFTABHUSEN H LAKSHMESHWAR	P
58	4JN19EC403	ANUSHA B V	P
59	4JN19EC404	ANUSHA G	P
60	4JN19EC406	KIRANKUMAR R	P
61	4JN19EC407	PALLAVI N S	P
62	4JN19EC408	POOJA A P	P
63	4JN19EC409	PREETHIKS	P
64	4JN19EC412	WILSON DSOUZA	P

Mr. Sachinkumar K.

Mr. Sachinkumar K.
Digital Design Engineer
Intel India Pvt. Ltd.

Bi zilv 121

Ms. Shwetha H.R. Assistant Professor, Department of ECE. JNNCE, Shivamogga

Dr. Sathyanarayana S.

Professor & Head Department of ECE JNNCE, Shivamogga